Reduced Switching Loss Using DC-Bus Clamping PWM Techniques for Nine-Switch Converter

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Abstract: The nine-switch converter (NSC) has been used in power quality conditioners and AC motor drives. However, it has not attracted much attention because of its amplitude, frequency and phase-shift limitations primarily due to sharing of its middle switches between two outputs. This sharing inherently imposes a constraint on its modulation index. To satisfy the modulation constraint and correctly synthesize the desired voltages, 'appropriate' DC offsets are often added to the phase voltage commands to decouple the converter's two outputs. This study proposes a new generalized carrier-based discontinuous PWM (or DC clamping) methodologies for the NSC with the ultimate goal of obtaining reduced switching losses while still maintaining its waveform quality and the realization of the converter full capacity. The mathematical formulations are validated with simulation results.

Keywords: nine-switch converter, reduced switch-count, ac motor drives, dc clamping pwm.

I. INTRODUCTION

In the classical pulse-width modulated voltage source inverters, two (2) main modulation techniques namely; Space Vector Pulse-Width Modulation (SV-PWM) and Carrier-Based Pulse-Width Modulation (CB-PWM) methods are used for controlling the magnitude and frequency of the output AC voltages. In both the SV-PWM and CB-PWM methods, voltage linearity, waveform quality (current ripple), and switching losses are all influenced by the choice of the zero-state placement [1]. Depending on the placement of these zero vectors, the modulation may be continuous or discontinuous. As discussed extensively by Hava et al. in [2] , the continuous PWM (CPWM) methods have superior performance in the low modulation range compared to the discontinuous PWM (DPWM) methods. The reverse is true in the high modulation region. However, each DPWM modulator's performance viz-a-viz switching losses, waveform quality, and voltage linearity characteristics are different in each DPWM method and the method of choice depends on the characteristics that are most critical to the designer.

Recently, some researchers have shown keen interest in the nine-switch converter (NSC) shown in Fig. 1. It has been used in independent control of two 3-phase AC loads [3]-[5] and in unified power quality conditioners [6]. The SV-PWM of the NSC has been investigated in [5], [7], and [8] whereas the CB-PWM methods are discussed in [8], [9]. The voltage harmonic performance of the NSC has been shown to be similar to that of its conventional two-level version [5]. The switching losses, too, per device are comparable except that in the NSC, the switching losses in the devices are not evenly shared. It is shown that the middle switches of the NSC are subjected to higher current stress and therefore more power losses than the top and bottom devices. This is a drawback as uneven distribution of heat leads to a lower rating for the converter.

Hereinafter, the upper portion of the NSC comprising the upper and middle switches (T_{ap}, T_{bp}, T_{cp} and T_{am}, T_{bm}, T_{cm}) is referred to as *NSC1* whereas the lower portion comprising the middle and lower switches (T_{am}, T_{bm}, T_{cm} and T_{an}, T_{bn}, T_{cn}) is *NSC2* as shown in Fig. 1.

In this paper, various DPWM methods of the NSC are proposed. Due to the DC clamping, switching losses would be reduced as compared to its continuous PWM method and consequently raise the power rating of the converter. Section II is used to introduce the PWM methods for the NSC. In Section III, the proposed generalized DC clamping method is outlined. This is followed by Simulation results and conclusions in Sections IV and V respectively.

II. NSC MODULATION METHODOLOGIES

The space vector diagram of the NSC is shown in Fig. 2 [7], [8]. It has 12 active and 3 zero space vectors that can be used to synthesize any desired 2 sets of 3-phase voltages. Using the space vector technique, the converter neutral voltages have been shown to be given by [8]:

$$V_{z1o} = \begin{pmatrix} \frac{V_{dc}}{2}(1\text{-}2\alpha) + V_{\max 1} + \\ \alpha(V_{\max 1} + V_{\max 2}) - \sim (V_{\min 1} + V_{\min 2}) \end{pmatrix} \quad (1a)$$

$$V_{z2o} = \begin{pmatrix} \frac{V_{dc}}{2}(2\beta - 1) - V_{\min 2} \\ -\beta(V_{\max 1} + V_{\max 2}) + \beta(V_{\min 1} + V_{\min 2}) \end{pmatrix} \quad (1b)$$

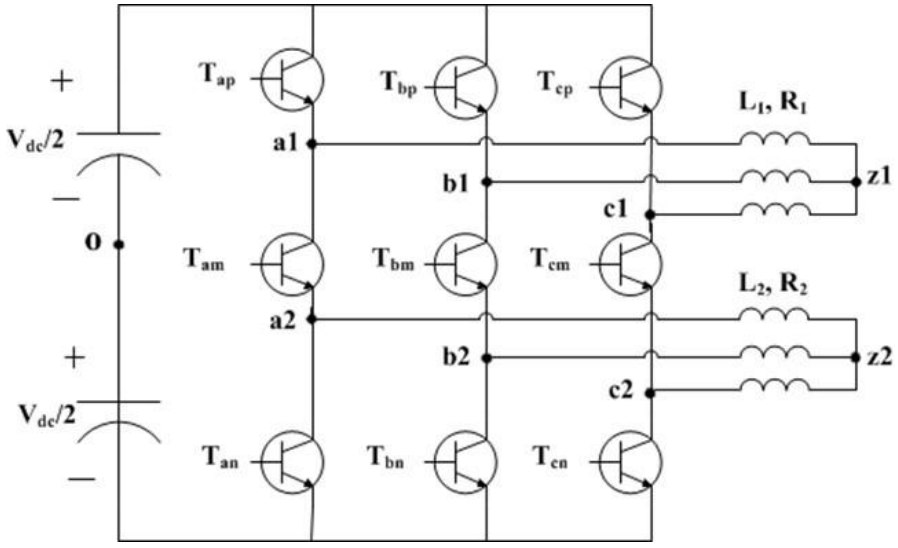


Figure 1: Topology of the nine-switch converter.

$$\text{where} \quad \begin{aligned} V_{\max 1} &= \max(V_{az1}, V_{bz1}, V_{cz1}), \\ V_{\min 1} &= \min(V_{az1}, V_{bz1}, V_{cz1}), \\ V_{\max 2} &= \max(V_{az2}, V_{bz2}, V_{cz2}), \\ V_{\min 2} &= \min(V_{az2}, V_{z2}, V_{cz2}) \end{aligned} ;$$

V_{jz1} and V_{jz2} are the phase voltages; $j = a, b, c$; α, β and γ are the distribution factors for the zero space vectors; V_{dc} is the DC-link voltage as shown in Fig. 1. In general, there are 3 zero vectors; and depending on the choice of the values for α, β and γ determines the DPWM method. Table I shows some proposed utilization of the 3 zero vectors. The sum of α, β and γ must however be less than or equal to unity. In Table I, a "0" means the associated zero vector has been eliminated and a "1" means the corresponding zero vector is being utilized.

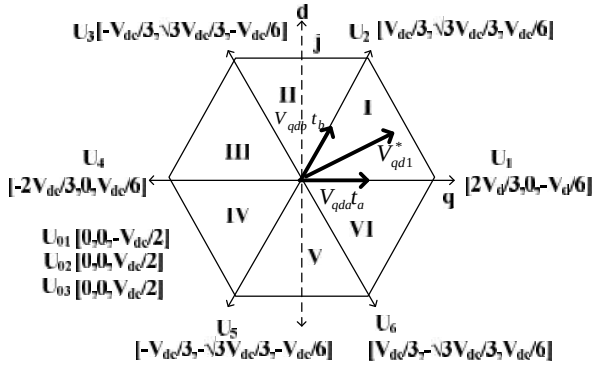
It can also be shown that the switching functions of the devices in a leg are related by (2) and the voltages between the converter legs and the mid-point, "O" of the DC-link capacitor are given by (3) as follows [8]:

$$\left.\begin{aligned} S_{ip} + S_{im}S_{in} &= 1, \\ S_{in} + S_{ip}S_{im} &= 1 \end{aligned}\right\} \tag{2}$$

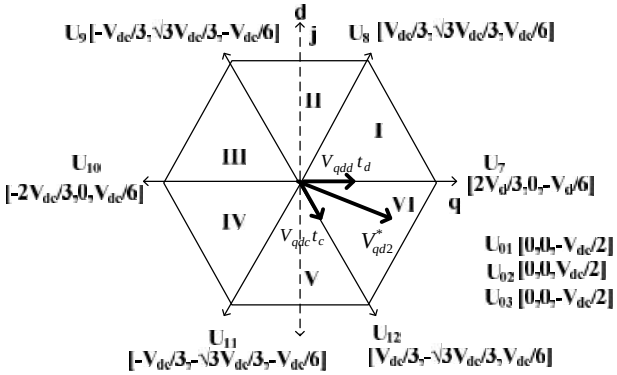
$$\left.\begin{aligned} V_{j0} &= V_{jn} + V_{n0} = V_{dc}(2S_{ip} - 1)/2, \\ V_{k0} &= V_{km} + V_{m0} = V_{dc}(1 - 2S_{in})/2 \end{aligned}\right\} \tag{3}$$

The expressions for the switching functions of the top and bottom devices can be approximated as [1]:

$$\left.\begin{aligned} S_{ip} &= 0.5(1 + M_{ip}) \\ S_{in} &= 0.5(1 + M_{in}) \end{aligned}\right\} \tag{4}$$



(a)



(b)

Figure 2: Space vector diagrams of nine-switch converter (a) *NSC1* output (b) *NSC2* output (c)

Substituting (4) into (3) the expressions for the modulation signals are given by:

$$\left.\begin{aligned} M_{ip} &= \frac{2V_{jz1}^{*}}{V_{dc}} + \frac{2V_{z1o}}{V_{dc}} \\ M_{in} &= -\frac{2V_{jz2}^{*}}{V_{dc}} - \frac{2V_{z2o}}{V_{dc}} \end{aligned}\right\} \quad (5)$$

where M_{ip}, M_{in} are respectively, the modulation signals of the upper and bottom devices. The expressions in (5) are compared with the high frequency carrier signals to produce the switching pulses as done in carrier-based PWM methods.

III. PROPOSED DISCONTINUOUS PWM SCHEMES

In discontinuous PWM methods, the zero sequence signals are used to modify the modulation signals clamping them to the positive or negative peak of the triangular carrier signal. The result is that the inverter phase legs are clamped to either the positive or negative DC rail for 120° portion of the fundamental period. In the most popular DPWM methods, the 120° clamping segment may be done in a single segment (120° DPWM) or divided into 2 or 4 separate segments (60° and 30° DPWM respectively).

Equation (1) represents the zero sequence voltages of the NSC. Variants of DPWMs may be achieved by eliminating either one or two of the three zero space vectors as shown in Table I. This may be done in two ways; eliminate the same zero vector(s) throughout a switching cycle or alternately eliminate different zero space vector(s) during the fundamental period. e.g., if only a single zero vector is to be applied, from Table I, either mode *a (i)*, or *a (ii)* or *a (iii)* only is used in a switching cycle but not a combination of them. In the second scenario of applying a single zero vector, *a (i)*, *a (ii)*, and *a (iii)* are alternately used within the time but alternates between all three zero vectors within the fundamental period. Equation (6) may be used to achieve this condition. However if the expression in (7) is used, one or two zero vectors are alternately eliminated within the switching period.

Table I: Zero voltage utilization

Mode	α	β	γ
a (i)	0	0	1
a (ii)	0	1	0
b(i)	0	1	1
a (iii)	1	0	0
b (ii)	1	0	1
b (iii)	1	1	0

$$\left.\begin{aligned} \sim &= 0.5[1+\mathrm{sgn}((\cos 3(\mu_1 t + ¢_1))], \\ &= 0.5[1+\mathrm{sgn}((\cos 3(\mu_2 t + ¢_2))](1-\sim) \\ \sim + \quad &+ ¥ = 1 \end{aligned}\right\} \quad (6)$$

$$\left.\begin{aligned} \sim &= 0.25[1+\mathrm{sgn}((\cos 3(\mu_1 t + ¢_1))], \\ &= 0.25[1+\mathrm{sgn}((\cos 3(\mu_2 t + ¢_2))], \\ \sim + \quad &+ ¥ = 1 \end{aligned}\right\} \quad (7)$$

In (6) and (7) sgn(X) is 1, 0 or -1 for $X > 0$, $X = 0$ and $X < 0$, respectively; ω_1, ω_2, are the frequencies of reference voltages of *NSC1* and *NSC2* respectively; δ_1 and δ_2 are their corresponding modulation angles. The modulation angle may be varied from $-\pi$ to $-\pi$ radians giving rise to infinite DPWM methods.

IV. SIMULATION RESULTS

Simulations were performed using Matlab/Simulink to validate the proposed PWM schemes. The simulation parameters are given in Table II.

Table II. Parameters of simulations and experimental setup

Parameter(s)	Value(s)
Phase 'a_1' V_1/V; f_1/Hz	$0.5V_{dc}/\sqrt{3}$; 60
Phase 'a_2' V_2/V; f_2/Hz	$0.5V_{dc}/\sqrt{3}$; 30
Switching Freq./kHz	1
V_{dc}/V	100
R_1/Ω; L_1/mH	2; 10
R_2/Ω; L_2/mH	2; 10

The DC-link voltage of 100 V is used and therefore $m_1 = m_2 = 1/\sqrt{3}$, (where m_1 = peak ($2V_{jz1}/V_{dc}$) and m_2 = peak ($2V_{jz2}/V_{dc}$) are the peaks of the reference modulation signals). The converter switching frequency chosen is 1 kHz.

Figs. 3 to 5 show the modulation signals of the proposed DPWM methods. In Fig. 3, when γ = 1, both top and bottom signals are clamped to the peak of the triangular carrier and therefore there are no

conduction losses in these clamped segments. However, if either $\alpha = 1$ or $\beta = 1$ as in Figs. 4(a) and 4(b), only one signal experiences the clamping. In other words, one set of modulation signals are continuous and the other discontinuous.

Fig. 5 shows the modulation signals when two of the 3 zero space vectors eliminated alternately eliminated during the switching cycle. Fig. 5 with Figs. 3 and 4 show that DC clamping can be applied to both NSC1 and NSC2 only if at least two zero vectors are eliminated alternately during a switching cycle. Figs. 6 and 7 illustrates respectively, the phase voltages and currents of NSC1 and NSC2 as well as their corresponding harmonic spectra. For lack of space, only the voltages and currents for corresponding to Fig. 5(b) are presented. There no low order harmonics and the dominant harmonics are centered around the converter switching frequency (1 kHz). The harmonic spectra for both voltages and currents shows the desired voltages have been synthesized correctly using the proposed algorithm.

V. CONCLUSIONS

Different DC-clamping PWM methodologies for the nine-switch converter have been proposed. The generalized neutral voltages for the NSC have been used to derive the generalized discontinuous PWM of the nine switch converter for the first time in this paper. Simulation results show that the waveform quality is comparable to the classical 2-level converter. Switching losses can be significantly reduced due to the clamping. It has also been shown, in this paper that, in fact, with an appropriate elimination of zero vectors, the converter's two sets of reference voltages may be obtained using a combination of both continuous and discontinuous PWM methods. Simulation results show that two sets of 3-phase voltages have been correctly synthesized by the proposed discontinuous PWM modulation techniques.

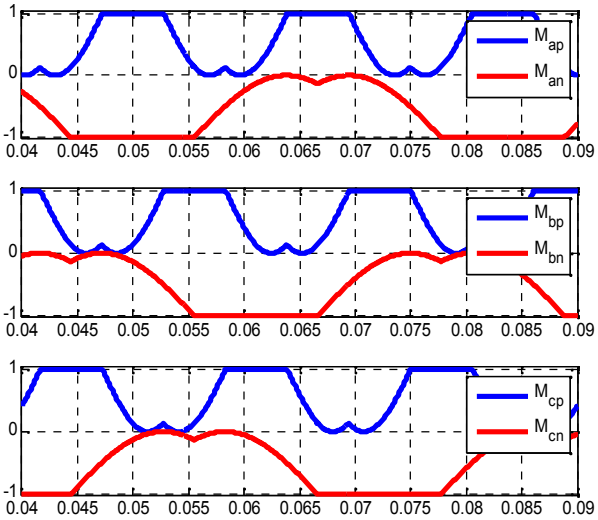
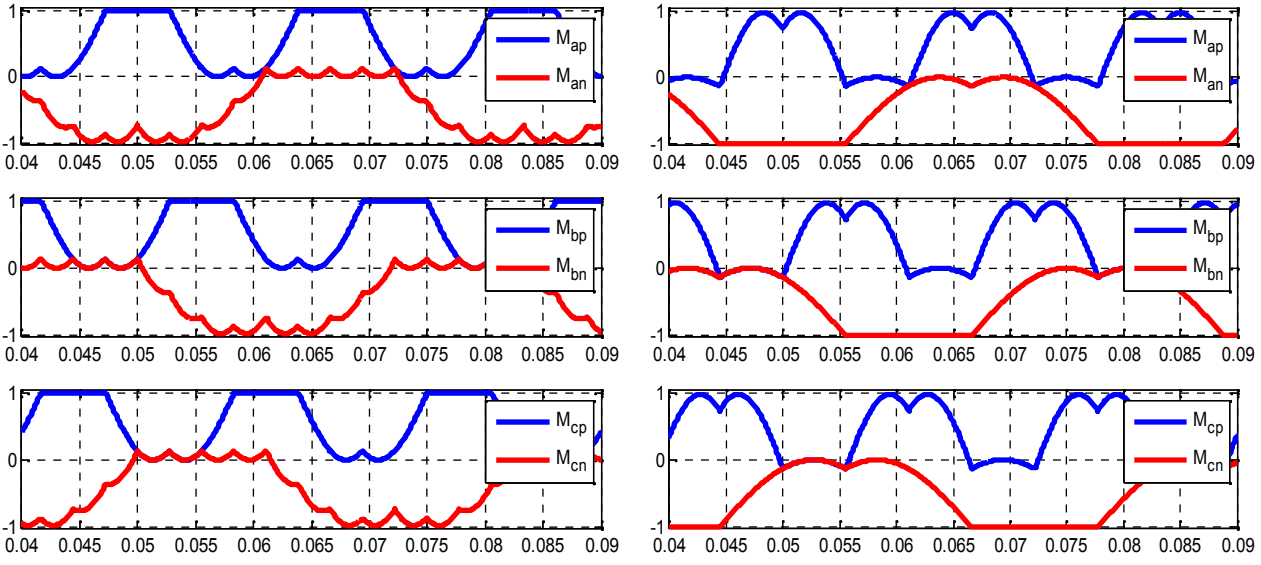


Figure 3: DPWM phases *abc* modulation signals with $\alpha = 0$, $\beta = 0$, $\gamma = 1$ when $f_1 = 60$ Hz, $f_2 = 30$ Hz, $m_1 = m_2 = 1/\sqrt{3}$.



(b) (c)

Figure 4: DPWM phases *abc* modulation signals with (a) $\alpha = \gamma = 0$, $\beta = 1$, and (b) $\alpha = 1$, $\beta = \gamma = 0$, when $f_1 = 60$ Hz, $f_2 = 30$ Hz, $m_1 = m_2 = 1/\sqrt{3}$;

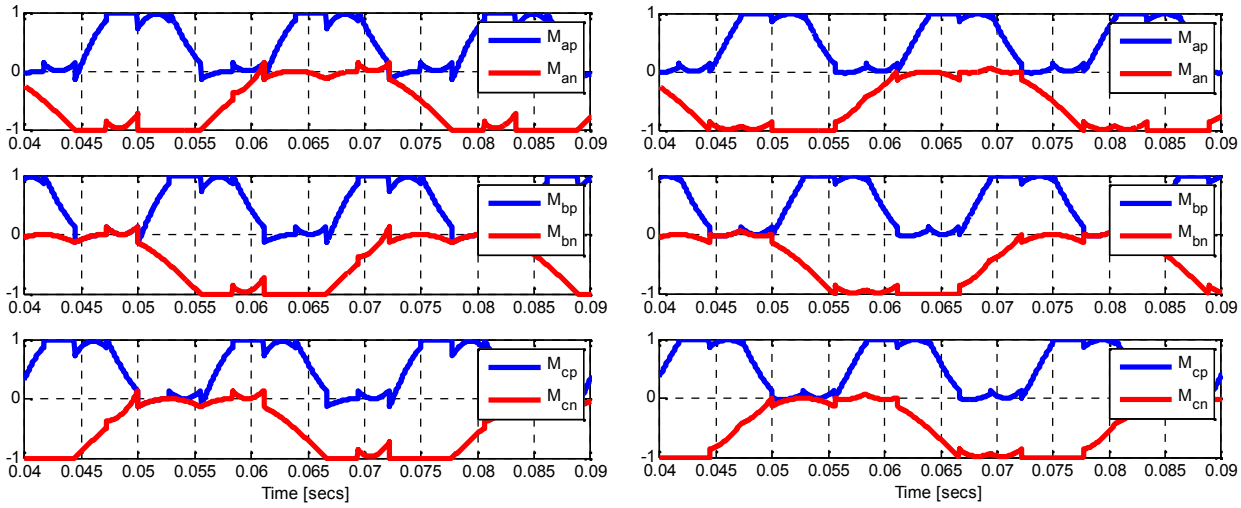


Figure 5: DPWM Modulation signals using (a) only one of α , β or , γ , and (b) only one or two of α, β and γ alternately in a switching cycle when f_1 = 60Hz, f_2 = 30Hz, $m_1 = m_2 = 1/\sqrt{3}$, $\delta_1 = \delta_2 = 0^o$.

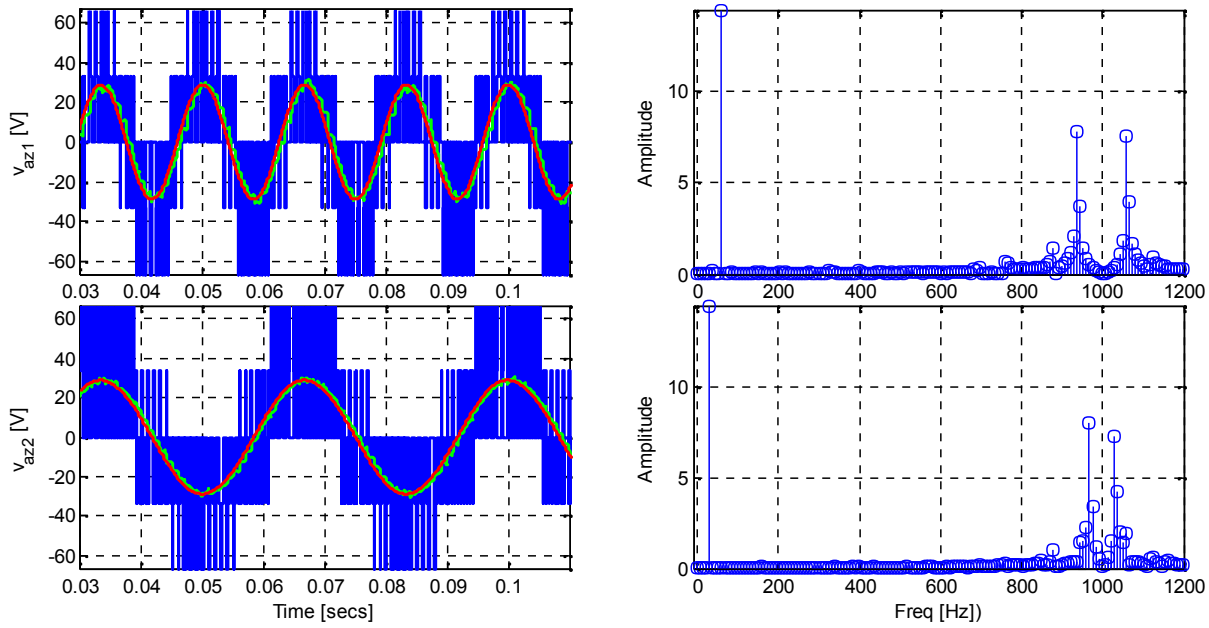


Figure 6: NSC 3- phase voltages and harmonic spectra *NSC1* output (top) and (d) *NSC2* output (bottom) using only one of α, β or γ alternately in a switching cycle with f_1 = 60 Hz, f_2 = 30 Hz, $m_1 = m_2 = 1/\sqrt{3}$, , $\delta_1 = \delta_2 = 0^o$

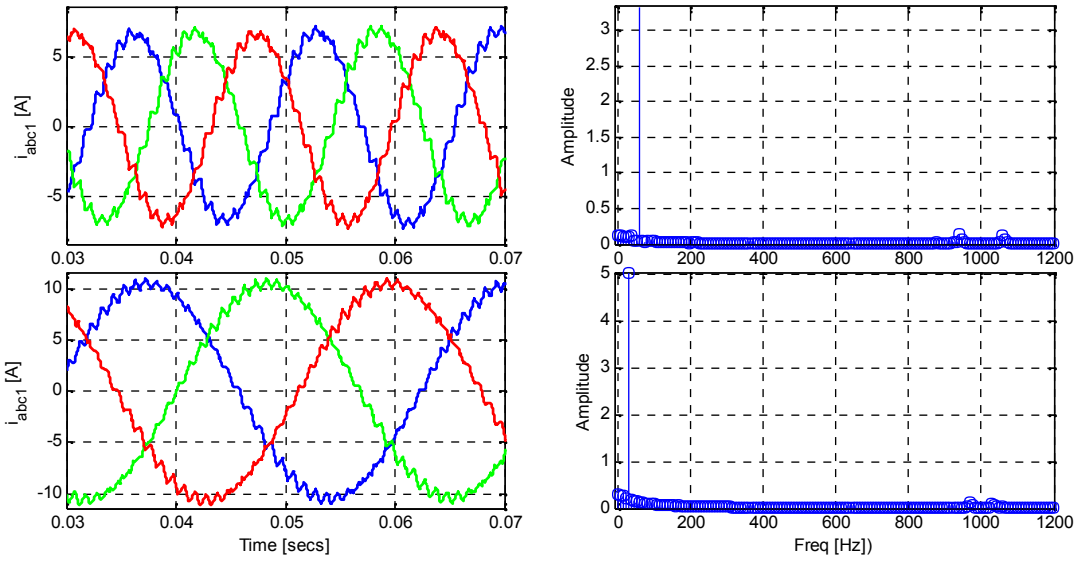


Figure 7: NSC 3- phase currents and harmonic spectra for *NSC1* output (top) and *NSC2* output (bottom) using only one of α , β or , γ alternately in a switching cycle with f_1 = 60 Hz, f_2 = 30 Hz, $m_1 = m_2 = 1/\sqrt{3}$, , $\delta_1 = \delta_2 = 0^o$

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